THAT WHICH IS CLAIMED IS:

1. An integrated circuit device comprising:

a substrate;

a first insulation layer on the substrate;

a contact pad disposed in the first insulation layer in direct contact with the substrate;

a second insulation layer on the first insulation layer;

a conductive pattern in the second insulation layer; and

a conductive plug extending through the second insulation layer to contact the contact pad and self-aligned to the conductive pattern.

2. The device according to Claim 1, wherein the second insulation layer comprises an oxide, and wherein the conductive pattern comprises tungsten.

3. The device according to Claim 1, further comprising an insulation film separating the conductive pattern and the conductive plug.

4. The device according to Claim 3, wherein the insulation film comprises silicon oxide and/or silicon nitride.

5. The device according to Claim 4, wherein the insulation film has a thickness of about 50Å to about 600Å.

6. The device according to Claim 1, wherein the conductive pattern comprises a bit line.

7. The device according to Claim 1, wherein the conductive pattern comprises a damascene pattern disposed in a trench in the second insulation layer.

8. The device according to Claim 1:

wherein the first insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the second insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material.

9. The device according to Claim 1, further comprising a glue layer disposed between the conductive pattern and the second insulation layer.

10. The device according to Claim 9, wherein the glue layer comprises titanium nitride, tantalum nitride or boron nitride.

11. The device according to Claim 9, wherein the glue layer has a thickness less than about 300Å.

12. The device according to Claim 1, wherein the conductive pattern comprises tungsten, tantalum nitride, titanium nitride, cobalt, nickel and/or aluminum.

13. The device according to Claim 1, further comprising a third insulation layer on the second insulation layer and the conductive pattern, and wherein the conductive plug extends through the second and third insulation layers.

14. The device according to Claim 13, wherein the third insulation layer comprises a silicon oxide, a high density plasma oxide, a tetraethyl ortho-silicate, a middle temperature oxide and/or a high temperature oxide, a polysilazane, a flowable oxide and/or a black diamond material.

15. The device according to Claim 1:

wherein the conductive pattern comprises tungsten, tantalum nitride, aluminum, nickel, or cobalt; and

wherein the conductive plug comprises tungsten, titanium nitride, tantalum nitride and/or polysilicon.

16. An integrated circuit memory device comprising:

a substrate having a source/drain region therein;

a first insulation layer on the substrate;

a storage node contact pad disposed in the first insulation layer and directly contacting the source/drain region;

a second insulation layer on the first insulation layer;

first and second damascene bit lines disposed in respective trenches in the second insulation layer on opposite sides of the storage node contact pad;

a conductive plug extending through the second insulation layer between the first and second damascene bit lines to contact the storage node contact pad, the conductive plug self-aligned to the first and second bit lines; and

a capacitor disposed on the conductive plug.

17. The memory device according to Claim 16, wherein the second insulation layer comprises an oxide, and wherein the first and second bit lines each comprise tungsten.

18. The memory device according to Claim 16, further comprising an insulation film separating each of the first and second bits lines from the conductive plug.

19. The memory device according to Claim 16:

wherein the first insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the second insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide,

a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material.

20. The memory device according to Claim 16, further comprising respective glue layers disposed between respective ones of the first and second bit lines and the second insulation layer.

21. The memory device according to Claim 20, wherein the glue layers each comprises titanium nitride, tantalum nitride or boron nitride.

22. The memory device according to Claim 16, wherein the first and second bit lines each comprises tungsten, tantalum nitride, titanium nitride, cobalt, nickel and/or aluminum.

23. The memory device according to Claim 16, further comprising a third insulation layer on the second insulation layer and the first and second bit lines, wherein the conductive plug extends through the second and third insulation layer, and wherein the capacitor is disposed on the third insulation layer.

24. The memory device according to Claim 23, wherein the third insulation layer comprises a silicon oxide, a high density plasma oxide, a tetraethyl ortho-silicate, a middle temperature oxide and/or a high temperature oxide, a polysilazane, a flowable oxide and/or a black diamond material.

25. The memory device according to Claim 16:

wherein the first and second bit lines each comprise tungsten, tantalum nitride, aluminum, nickel, or cobalt; and

wherein the conductive plug comprises tungsten, titanium nitride, tantalum nitride and/or polysilicon.

26. A method of fabricating an integrated circuit device, the method comprising:

forming a first insulation layer on a substrate;

forming a contact pad in the first insulation layer in direct contact with the substrate;

forming a second insulation layer on the first insulation layer;

forming a conductive pattern in the second insulation layer; and

forming a conductive plug extending through the second insulation layer to contact the contact pad and self-aligned to the conductive pattern.

27. The method according to Claim 26, wherein the second insulation layer comprises an oxide, and wherein the conductive pattern comprises tungsten.

28. The method according to Claim 26, wherein forming a conductive plug is preceded by forming an insulation film on a sidewall of the conductive pattern.

29. The method according to Claim 28, wherein the insulation film comprises silicon oxide and/or silicon nitride.

30. The method according to Claim 29, wherein the insulation film has a thickness of about 50Å to about 600Å.

31. The method according to Claim 26, further comprising forming a third insulation layer on the second insulation layer and the conductive pattern, and wherein forming a conductive plug extending through the second insulation layer to contact the contact pad and self-aligned to the conductive pattern comprises forming a conductive plug that extends through the second and third insulation layers.

32. The method according to Claim 31:

wherein the first insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the second insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the third insulation layer comprises a silicon oxide, a high density plasma oxide, a tetraethyl ortho-silicate, a middle temperature oxide and/or a high temperature oxide, a polysilazane, a flowable oxide and/or a black diamond material.

33. The method according to Claim 31, wherein forming a conductive plug that extends through the second and third insulation layers comprises:

etching the second and third insulation layers to form a contact hole that exposes the contact pad and a sidewall of the conductive pattern;

forming an insulation film lining the contact hole;

removing a portion of the insulation film on the contact pad to expose the contact pad; and

forming the conductive plug in the contact hole on the exposed contact pad.

34. The method according to Claim 33, wherein forming the conductive plug in the contact hole comprises:

depositing a conductive material on the substrate, filling the contact hole; and

planarizing the substrate to form the conductive plug.

35. The method according to Claim 26, wherein forming a conductive pattern comprises:

forming a trench in the second insulation layer;

depositing a conductive material on the substrate and in the trench; and

planarizing the substrate to form the conductive pattern in the second insulation layer.

36. The method according to Claim 35, wherein depositing a conductive material is preceded by forming a glue layer in the trench.

37. The method according to Claim 36, wherein the glue layer comprises titanium nitride, tantalum nitride or boron nitride.

38. The method according to Claim 36, wherein the glue layer has a thickness less than about 300Å.

39. The method according to Claim 26, wherein the conductive pattern comprises tungsten, tantalum nitride, titanium nitride, cobalt, nickel and/or aluminum.

40. The method according to Claim 26:

wherein the conductive pattern comprises tungsten, tantalum nitride, aluminum, nickel, or cobalt; and

wherein the conductive plug comprises tungsten, titanium nitride, tantalum nitride and/or polysilicon.

41. A method of fabricating an integrated circuit memory device, the method comprising:

forming a source/drain region in a substrate;

forming a first insulation layer on the substrate;

forming a storage node contact pad in the first insulation layer and in contact with the source/drain region;

forming a second insulation layer on the first insulation layer;

forming first and second damascene bit lines in respective trenches in the second insulation layer on opposite sides of the storage node contact pad;

forming a conductive plug extending through the second insulation layer between the first and second damascene bit lines to contact the storage node contact pad, the conductive plug self-aligned to the first and second bit lines; and

forming a capacitor on the conductive plug.

42. The method according to Claim 41, wherein forming a conductive plug is preceded by forming a third insulation layer on the second insulation layer and the first and second bit lines, wherein forming a conductive plug comprise forming a conductive plug that extends through the second and third insulation layer, and wherein forming a capacitor comprises forming the capacitor on the third insulation layer.

43. The method according to Claim 42, wherein forming a conductive plug that extends through the second and third insulation layer comprises:

etching the second and third insulation layers to form a contact hole that exposes the storage node contact pad and sidewalls of the first and second bit lines;

forming an insulation film lining the contact hole;

removing a portion of the insulation film on the storage node contact pad to expose the storage node contact pad; and

forming the conductive plug in the contact hole on the exposed storage node contact pad.

44. The method according to Claim 43, wherein forming the conductive plug in the contact hole comprises:

depositing a conductive material on the substrate, filling the contact hole; and

planarizing the substrate to form the conductive plug.

45. The method according to Claim 42:

wherein the first insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material;

wherein the second insulation layer comprises a silicon oxide, a high density plasma oxide, a high temperature oxide, a middle temperature oxide, a tetraethyl ortho-silicate, a polysilazane, a flowable oxide and/or a black diamond material; and

wherein the third insulation layer comprises a silicon oxide, a high density plasma oxide, a tetraethyl ortho-silicate, a middle temperature oxide and/or a high temperature oxide, a polysilazane, a flowable oxide and/or a black diamond material.

46. The method according to Claim 41, wherein the second insulation layer comprises an oxide, and wherein the first and second bit lines each comprise tungsten.

47. The method according to Claim 41, wherein forming a conductive plug is preceded by forming an insulation film on sidewalls of the first and second bit lines.

48. The method according to Claim 41, wherein forming first and second bit lines is preceded by forming respective glue layers in respective ones of the trenches.

49. The method according to Claim 48, wherein the glue layers each comprise titanium nitride, tantalum nitride or boron nitride.

50. The method according to Claim 41, wherein the first and second bit lines each comprise tungsten, tantalum nitride, titanium nitride, cobalt, nickel and/or aluminum.

51. The method according to Claim 41:

wherein the first and second bit lines each comprise tungsten, tantalum nitride, aluminum, nickel, or cobalt; and

wherein the conductive plug comprises tungsten, titanium nitride, tantalum nitride and/or polysilicon.